AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Previously presented) A method of managing power consumption in a computing system having a plurality of performance states, including a maximum performance state and a plurality of other performance states that provide successively less performance capability for an integrated circuit, the method comprising:

determining utilization of the integrated circuit; and

each time the computing system determines that a higher performance state is required based on the determined utilization while in each of the other performance states, changing to a predetermined performance state, skipping all intermediate performance states between a current performance state and the predetermined performance state.

2. (Currently amended) The method as recited in claim 1 wherein the predetermined performance state is [[a]] the maximum performance state.

3. (Original) The method as recited in claim 1 wherein the predetermined performance state is a near maximum performance state.

4. (Previously presented) The method as recited in claim 1 further comprising:

comparing the determined utilization to a threshold utilization value to determine if a higher performance state is required;

comparing the integrated circuit utilization to a second threshold utilization value; and

if the integrated circuit utilization is below the second threshold utilization value, always entering a next lower performance state as a next performance state.

5. (Previously presented) The method as recited in claim 1 further comprising:

comparing the determined utilization to a threshold utilization value to determine if a higher performance state is required;

comparing the integrated circuit utilization to a second threshold utilization value;

if the integrated circuit utilization is below the second threshold utilization value,

entering a lower performance state as a next performance state, the lower performance state being determined according to integrated circuit utilization.

6. (Original) The method as recited in claim 4 wherein the performance state is lowered by reducing at least one of the voltage and frequency.

7. (Original) The method as recited in claim 1 wherein the performance state is reduced by reducing both voltage and clock frequency of the integrated circuit.

8. (Original) The method as recited in claim 1 wherein determining the utilization is done periodically.

9. (Original) The method as recited in claim 1 wherein the integrated circuit includes a central processing unit.

10. (Previously presented) A computing system comprising:

an integrated circuit having multiple performance states including a maximum performance state and multiple lesser performance states;

wherein the computing system is operable to determine utilization of the integrated circuit; and

wherein the computing system is operable, each time the computing system determines that a higher performance state is required while in each of the multiple lesser performance states, to change to the maximum performance state, skipping any intermediate performance states between a current one of the multiple lesser performance states and the maximum performance state.

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Original) The computing system as recited in claim 10 wherein each of the performance states is defined by a unique voltage and frequency combination.

15. (Original) The computing system as recited in claim 10 wherein the integrated circuit includes a central processing unit (CPU).

16. (Previously presented) The computing system as recited in claim 10 further comprising:

an instruction sequence operable to change operation of the integrated circuit from the current performance state to a target lower performance state in response to a determination that the utilization is below a second threshold utilization value.

17. (Original) The computing system as recited in claim 16 wherein the target lower performance state is one of a plurality of lower performance states determined according to CPU utilization.

18. (Original) The computing system as recited in claim 16 wherein the lower performance state is always a next lower performance state.

19. (Previously presented) A computing system comprising:

an integrated circuit having multiple performance states;

means for determining utilization of the integrated circuit; and

means for changing, while in each of the performance states other than a maximum performance state, from a current performance state to the maximum performance state, skipping all intermediate performance states between the current performance state and the maximum performance state, each time the computing system determines that a higher performance is required based on the determined utilization.

20. (Canceled)

21. (Original) The computing system as recited in claim 19 further comprising:

means for determining that the utilization is below a second threshold value and for always changing operation of the integrated circuit from the current performance state to a next lowest performance state in response to a determination that the utilization is below a second threshold utilization value.

22. (Original) The computing system as recited in claim 19 further comprising:

means for determining that the utilization is below a second threshold value and for changing operation of the integrated circuit from the current performance state to a lower performance state in response to a determination that the utilization is below a second threshold utilization value, the lower performance state being determined according to the integrated circuit utilization.

23. (Previously presented) A computer program product encoded on a computer readable medium comprising:

a first instruction sequence operable on a processor having a plurality of lower performance states and a maximum performance state, to determine utilization of the processor; and

a second instruction sequence operable to change from a current one of the lower performance states to the maximum performance state, skipping any performance state between the current one of the lower performance states and the maximum performance state, in response to each determination that a performance increase is required while in each of the lower performance states.

24. (Previously presented) The computer program product as recited in claim 23, wherein the computer readable medium is selected from the set of a disk, tape or other magnetic, optical, or electronic storage medium.

25. (Canceled)

26. (Original) The computer program product as recited in claim 23 further comprising:

a third instruction sequence operable to change operation of the processor from the current performance state to a target lower performance state in response to a determination that the utilization is below a second threshold utilization value.

27. (Original) The computer program product as recited in claim 26 wherein the target lower performance state is one of a plurality of lower performance states determined according to CPU utilization.

28. (Original) The computer program product as recited in claim 26 wherein the lower performance state is always a next lower performance state.

29. (Canceled)

30. (Canceled)

31. (Canceled)

32. (Canceled)